IFW AF 2823

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rich Fogal Tracy Reynolds Timothy Cowles	§	Group Art Unit: 2823
	§	Examiner: Khiem D. Nguyen
Serial No.: 09/945,084	§	Docket No.: 2001-0128.00
Filed: August 30, 2001	§	Confirmation No.: 3141
For: **METHOD AND APPARATUS FOR CIRCUIT COMPLETION THROUGH THE USE OF BALL BONDS OR OTHER CONNECTIONS DURING THE FORMATION OF A SEMICONDUCTOR DEVICE**	§	

Mail Stop Appeal Brief - Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing (37 CFR §1.8)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on the date below:

May 23, 2005 (Date) Merri Helm (Signature)

SUBMISSION OF BRIEF ON APPEAL

Please enter this Appeal Brief in response to the Examiner's Final Office Action mailed December 23, 2004 as paper no. 121704 and the Applicants' Notice of Appeal mailed March 23, 2005.

05/26/2005 AWONDAF1 00000048 133092 09945084
01 FC:1402 500.00 DA

TABLE OF CONTENTS

Page

I. Real Party In Interest

The applicants, Rich Fogel, Tracy Reynolds, and Timothy Cowles, have assigned their interest in this application to Micron Technology, Inc. as evidenced by the recordation on February 4, 2002 at reel/frame 012553/0258.

II. Related Appeals And Interferences

No known related appeals or interferences are pending.

III. Status Of The Claims

Claims 1-46 have been presented during prosecution of the application under appeal;

Claims 1-32 have been canceled, and;

Claims 33-46 are pending, rejected, and appealed.

IV. Status Of The Amendments

No amendment has been filed by the applicants for the above-captioned case subsequent to the final rejection of December 23, 2004.

V. Summary Of The Claimed Subject Matter

The present invention addresses a method for completing a circuit during the formation of a semiconductor device (page 7 lines 9-18). The embodiment of claim 33 (page 9 line 21 - page 10 line 20 in conjunction with FIG. 8) comprises forming a first circuit 82 and a second circuit 80 on a semiconductor wafer substrate assembly. A first conductor 86 connected to the first semiconductor circuit 82 is formed, and a second conductor 84 connected to the second semiconductor circuit 80 is formed. The first conductor 86 is electrically separated from the second conductor 84 such that the first 82 and second 80 circuits are sufficiently isolated to provide protection to the second circuit 80. With the first and second circuits electrically separate from each other, an electrical operation is performed on the first circuit 82 with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other (page 10 lines 1-3 and 13-20). Subsequent to performing the electrical operation on the first circuit, the first and second conductors are shorted together to electrically couple the first and second circuits (page 10 lines 19-20). Subsequent to shorting the first and second conductors together, the semiconductor wafer substrate assembly is encapsulated (page 8 lines 8-12).

Dependent claim 34, and analogous claims 39 and 44, recite the use of a ball bond to electrically short the first and second conductors together (page 10 lines 19-20).

Dependent claim 35, and analogous claims 40 and 45, recite that the circuits are fabricated such that the semiconductor device is inoperative when the first and second conductors remain electrically separate or unbridged (page 11 lines 1-5).

Dependent claim 36, and analogous claims 41 and 46, recite the attachment of the semiconductor wafer substrate assembly to a lead frame subsequent to shorting the first and second conductors together (original claim 7, for example).

The embodiment of independent claim 37 recites a method of manufacturing a memory device comprising forming a plurality of primary (page 9 line 22

"malfunctioning rows or columns") and redundant memory cell locations, and forming antifuse circuitry (page 10 lines 13-18 and FIG. 8) which allows selection of the redundant memory cell locations. Voltage sensitive circuitry (page 9 line 21- page 10 line 3, FIG. 8 80, transistor "T1" for example) is formed on the semiconductor wafer substrate assembly, and a first conductor 86 is formed which is electrically connected with the antifuse circuitry 82. A second conductor 84 is formed which is electrically connected with the voltage sensitive circuitry 80, wherein the first 86 and second 84 conductors are electrically separated from each other. While the first and second conductors are electrically separated, a voltage is applied to the antifuse circuitry to program the antifuse circuitry, wherein the voltage applied is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected (page 9 line 2- page 10 line 20). Subsequent to programming the antifuse circuitry, the first conductor is electrically shorted with the second conductor (page 10 lines 19-20).

Dependent claims 38 and 43 recite encapsulating the antifuse circuitry, the voltage sensitive circuitry, the first conductor subsequent to electrically shorting the first conductor with the second conductor (claim 38) or encapsulating the first and second circuits and the common conductor subsequent to bridging the physical opening (claim 43). See page 8 lines 8-12.

The embodiment of independent claim 42 recites a method of manufacturing a memory device comprising fabricating first and second circuits on a semiconductor wafer substrate assembly, wherein the first and second circuits are adapted to be electrically connected through a common conductor. The common conductor is fabricated with a physical opening to provide an open circuit between the first and second circuits, such that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a voltage applied to the second circuit. The voltage is sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged. The voltage is applied to the second circuit, and subsequent to applying the voltage to the second circuit, the physical opening of the common conductor is bridged to electrically connect the first and second circuits together. See page 9 line 21-page 10 line 20.

VI. Ground Of Rejection To Be Reviewed On Appeal

Claims 33-35, 37-40, and 42-45 stand rejected under 35 USC §103(a) over JP 6-232537.

Claims 36, 41, and 46 stand rejected under 35 USC §103(a) over JP 6-232537 and AAPA (¶ [0010]) in combination.

VII. Argument

A. Rejection of claims under 35 USC §103(a) over JP 6-232537

The Examiner has rejected claims 33-35, 37-40, and 42-45 under 35 USC §103(a) as being unpatentable over JP 6-232537.

JP 6-232537 discloses a method which allows accurate trimming of a resistor independent of the circuit to which the resistor is attached. If the resistor is not separated from the circuit and from other resistors in the circuit, it can be trimmed but the trimming is not as exact (translation, ¶[0001] - [0004], specifically [0003]). JP 6-232537 concerns a particular method for connecting the circuit after trimming the resistor comprising the use of solder paste rather than using a soldering iron, which is excessively large for fine-pitch devices (¶[0007] - [0008])).

The present invention as claimed comprises novel and nonobvious differences over the invention of JP 6-232537. Claim 33 recites "...with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other...". Claim 42 comprises a similar recitation.

The translation of JP 6-232537 does not indicate how the resistor is trimmed, but does not teach that a voltage is applied to the resistor in order to trim the resistor. Thus the recitation from claim 33, and the similar recitation of claim 42, of "with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit *with a voltage*" is not met. In addition to omitting the application of a voltage to trim the resistor, JP 6-232537 particularly fails to address the application of a voltage which is "*sufficient to damage the second circuit* when applied to the first circuit with the first and second circuits electrically connected to each other." As JP 6-232537 does not teach or suggest all the claim limitations as required (MPEP §706.02(j)), independent claims 33 and 42, and rejected claims 34, 35, and 43-46 which depend therefrom are allowable under 35 USC §103(a) for this reason alone.

In the penultimate paragraph of page 7 of the final office action of December 23, 2004 (hereinafter "FOA"), the Examiner disagrees with the applicants' assertion that application of a voltage sufficient to damage the circuit is not taught but fails to indicate where JP 6-232537 supposedly teaches this limitation of the presently rejected claim. The Examiner states on page 2 of the FOA that this limitation is taught on pages 1-2 of the English translation, however the application of a voltage which would damage one circuit does not appear to be discussed. Some more particular indication of what part of the reference the Examiner is relying on to reject this limitation of claims 33 and 42 would appear reasonable so that the applicants have fair opportunity to fully respond to the rejection.

The Examiner suggests that claims 33 and 42 are properly rejected over JP 6-232537 because the disclosed process would require the same functional limitations as cited in the applicants' claimed invention since the same materials are treated in the same manner as the instant invention (FOA, page 3 lines 8-10 and page 6 lines 10-12). JP 6-232537 teaches that the trimming may be performed with the two circuit parts attached, however with the circuit parts attached "exact trimming becomes impossible" (¶ [0003] of the English translation). Thus it is evident that the trimming does not require a "voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other" as presently recited in claims 33 and 42, at least because trimming of the resistor is possible, albeit with decreased precision.

Regarding claims 34 and 44, the Examiner states that JP 6-232537 discloses shorting the first and second conductor together with a ball bond at FIG. 3c:14 and the English translation, page 1, ¶ [0005]. However, the reference appears to discuss printing soldering paste to the electrodes, then heating and fusing the soldering paste to result in a conductor bridging the two electrodes.

Regarding claims 35 and 45, the Examiner states that JP 6-232537 discloses that the first and second circuits are fabricated such that the "memory device" is inoperative if the first and second conductors remain electrically separate subsequent to encapsulation in the English translation at pages 1-2 and FIGS. It is not evident where JP 6-232537 discusses or suggests an inoperative device if the first and second conductors remain electrically separate, and it is not evident that the "hybrid IC" of JP 6-232537 would not function properly if the connection is not made.

It should be noted that while the Examiner states that JP 6-232537 discusses the formation of a "memory device," the reference does not appear to recite the manufacture of such a device. JP 6-232537 does recite the formation of a "hybrid IC" at ¶ [0001]. Although neither claim 35 nor claim 33 from which claim 35 depends recites the method performed on a "memory device," the omission of a "memory device" is relevant for subsequent claims, such as claims 37-46.

Regarding claim 37, the Examiner states that JP 6-232537 discloses a method of manufacturing a "memory device comprising forming a plurality of primary and redundant memory cell locations, forming antifuse circuitry which allows selection of the redundant memory cell locations; forming voltage sensitive circuitry on the semiconductor wafer substrate assembly, forming a first conductor electrically connected with the antifuse circuitry, applying a voltage to the antifuse circuitry to program the antifuse circuitry wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected, and subsequent to programming the antifuse circuitry, electrically shorting the first conductor with the second conductor.

The Examiner has not specifically pointed out where each of these elements are described by JP 6-232537, however it is not evident from the translation supplied by the Examiner that JP 6-232537 comprises any of the following features: a memory device, primary and redundant memory cell locations (or any memory cell locations), forming antifuse circuitry, forming a first conductor electrically

connected with the antifuse circuitry, applying a voltage to the antifuse circuitry to program the antifuse circuitry, particularly a voltage which is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected, and programming the antifuse circuitry. Another translation of JP 6-232537 is attached hereto in the Evidence Appendix which also omits the features described above. The reference discusses the trimming of a resistor on a "hybrid IC."

Claim 37 recites "forming a plurality of primary and redundant memory cell locations; forming antifuse circuitry which allows selection of the redundant memory cell locations; forming voltage sensitive circuitry...; forming a first conductor electrically connected with the antifuse circuitry; forming a second conductor electrically connected with the voltage sensitive circuitry...; while the first and second conductors are electrically separated, applying a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected...". Because JP 6-232537 fails to teach, suggest, or even imply various claimed features such as "a redundant memory cell location," "antifuse circuitry," "a first conductor electrically connected with the antifuse circuitry," claim 37 and rejected claims 38-41 which depend therefrom are allowable over JP 6-232537 under 35 USC §103(a).

As discussed relative to the rejections of claims 33-35 and 42 over JP 6-232537 under 35 USC §103(a), JP 6-232537 fails to teach or suggest the similar recitation "...while the first and second conductors are electrically separated, applying a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductor are electrically connected." JP 6-232537 indicates less precise trimming of the resistor is possible when the circuits are connected. As claim 37 recites that such use "is sufficient to damage the voltage sensitive circuitry," and the resistor trimming of the reference is not sufficient to damage the circuitry, claim 37 and claims 38-41 which depend therefrom are further allowable over JP 6-232537 under 35 USC §103(a).

In the rejection of claim 38, the Examiner states that JP 6-232537 discusses encapsulating the antifuse circuitry and the voltage sensitive circuitry on page 2 of the English translation. However, it appears the translation fails to disclose encapsulation, antifuse circuitry, and voltage sensitive circuitry, as well as encapsulation of the antifuse circuitry and the voltage sensitive circuitry, and doing so subsequent to electrically shorting the first conductor with the second conductor.

With regard to claim 39, the Examiner states that the cited reference recites a ball bond at ¶[0005]. However, the cited location discusses the formation of a solder paste which is heated to result in a conductor, and does not appear to disclose the use of a ball bond as suggested by the Examiner.

The Examiner states with regard to claim 40 that JP 6-232537 at pages 1-2 of the English translation recites fabricating antifuse circuitry and voltage sensitive circuitry such that the memory device is inoperative if the first and second conductors remain electrically separated. However, the reference does not appear to teach or suggest antifuse circuitry, voltage sensitive circuitry, circuit inoperability if the circuit portions remain separated, or a memory device.

Because JP 6-232537 fails to teach or suggest all the claim limitations as required (MPEP §706.02(j)), claims 33-35, 37-40, and 42-45 are allowable over JP 6-232537 under 35 USC §103(a). The Examiner's rejections of claims 33-35, 37-40, and 42-45 under 35 USC §103 over JP 6-232537 are respectfully traversed.

Claims 36, 41, and 46 have been rejected under 35 USC §103(a) as being unpatentable over JP 6-232537 in view of the applicants' admitted prior art, specifically ¶[0010] of page 4 (AAPA). It is submitted that the independent claims from which claims 36, 41, and 46 depend comprise novel and nonobvious differences over JP 6-232537, and therefore claims 36, 41, and 46 are allowable over JP 6-232537 and AAPA.

Because JP 6-232537 and AAPA in combination fail to teach or suggest all the claim limitations as required (MPEP §706.02(j)), the rejected claims are allowable over JP 6-232537 and AAPA in combination. The Examiner's rejections of claims 36, 41, and 46 under 35 USC §103 over JP 6-232537 are respectfully traversed.

Any claims not individually addressed are allowable at least because they depend from an allowable base claim. Thus it is submitted that all of claims 33-35, 37-40, and 42-45 are allowable over JP 6-232537 under 35 USC §103(a).

B. Conclusion

For the foregoing reasons, the applicants submit that claims 33-46 are clearly not anticipated by the disclosure of the cited references, which do not render the method of the applicants' invention obvious. Accordingly, applicants respectfully request the reversal of the Examiner's rejection of claims 33-46.

Respectfully submitted,

Kevin D. Martin
Agent for Applicant
Registration No. 37,882
Micron Technology, Inc.
Mail Stop 1-525
8000 S. Federal Way
Boise, ID 83716
Ph: (208) 368-4516
FAX: (208) 368-5606
e-mail: kmartin@micron.com

Claims Appendix

33. A method of manufacturing a semiconductor device, comprising:

forming a first circuit and a second circuit on a semiconductor wafer substrate assembly;

forming a first conductor connected to the first semiconductor circuit and a second conductor connected to the second semiconductor circuit, wherein the first conductor is electrically separated from the second conductor such that the first and second circuits are sufficiently isolated to provide protection to the second circuit;

with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other;

subsequent to performing the electrical operation on the first circuit, shorting the first and second conductors together to electrically couple the first and second circuits; and

subsequent to shorting the first and second conductors together, encapsulating the semiconductor wafer substrate assembly.

34. The method of claim 33 further comprising shorting the first and second conductors together with a ball bond.

35. The method of claim 33 wherein the first and second circuits are fabricated such that the semiconductor device is inoperative when the first and second conductors remain electrically separate subsequent to encapsulation.

36. (previously presented) The method of claim 33 further comprising:

providing a lead frame; and

subsequent to shorting the first and second conductors together, attaching the semiconductor wafer substrate assembly to the lead frame.

37. A method of manufacturing a memory device, comprising:

forming a plurality of primary and redundant memory cell locations;

forming antifuse circuitry which allows selection of the redundant memory cell locations;

forming voltage sensitive circuitry on the semiconductor wafer substrate assembly;

forming a first conductor electrically connected with the antifuse circuitry;

forming a second conductor electrically connected with the voltage sensitive circuitry, wherein the first and second conductors are electrically separated from each other;

while the first and second conductors are electrically separated, applying a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected; and

subsequent to programming the antifuse circuitry, electrically shorting the first conductor with the second conductor.

38. The method of claim 37 further comprising encapsulating the antifuse circuitry, the voltage sensitive circuitry, the first conductor, and the second conductor subsequent to electrically shorting the first conductor with the second conductor.

39. The method of claim 37 further comprising electrically shorting the first conductor with the second conductor using a ball bond.

40. The method of claim 37 wherein the antifuse circuitry and the voltage sensitive circuitry are fabricated such that the memory device is inoperative if the first and second conductors remain electrically separated.

41. The method of claim 37 further comprising:

providing a lead frame; and

subsequent to bridging the physical opening, attaching the semiconductor wafer substrate assembly to the lead frame.

42. A method of manufacturing a memory device comprising:

fabricating first and second circuits on a semiconductor wafer substrate assembly, wherein the first and second circuits are adapted to be electrically connected through a common conductor;

fabricating the common conductor with a physical opening to provide an open circuit between the first and second circuits, such that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a voltage applied to the second circuit which is sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged;

applying the voltage to the second circuit; and

subsequent to applying the voltage to the second circuit, bridging the physical opening of the common conductor to electrically connect the first and second circuits together.

43. The method of claim 42 further comprising encapsulating the first and second circuits and the common conductor subsequent to bridging the physical opening.

44. The method of claim 42 further comprising bridging the physical opening with a ball bond.

45. The method of claim 42 wherein the first and second circuits are fabricated such that the memory device is inoperative if the physical opening remains unbridged.

46. The method of claim 42 further comprising:

providing a lead frame; and

subsequent to bridging the physical opening, attaching the semiconductor wafer substrate assembly to the lead frame.

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL for FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500

Complete if Known	
Application Number	09/945,084
Filing Date	August 30, 2001
First Named Inventor	Rich Fogal et al.
Examiner Name	Khiem D. Nguyen
Art Unit	2823
Attorney Docket No.	2001-0128.00/US

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify) : _____

☒ Deposit Account Deposit Account Number: 13-3092 Deposit Account Name: Micron Technology, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) Under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee($)	Fee($)	Fee($)	Fee($)	Fee($)	Fees Paid ($)
Utility	300	150	500	250	200	100	____
Design	200	100	100	50	130	65	____
Plant	200	100	300	150	160	80	____
Reissue	300	150	500	250	600	300	____
Provisional	200	100	0	0	0	0	____

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee($)		Fee Paid ($)
____	-20 or HP=	____	x	____	=	____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims		Fee($)		Fee Paid ($)
____	- 3 or HP=	____	x	____	=	____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
____	____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)	Fee Paid ($)
____	- 100 =	____	/ 50 =	____	(round **up** to a whole number) x		= ____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	____
Other (e.g., late filing surcharge) : Brief on Appeal	500

SUBMITTED BY

Signature	Kevin D Martin	Registration No. (Attorney/Agent) 37,882	Telephone 208-368-4516
Name (Print/Type)	Kevin D. Martin		Date May 23, 2005

Evidence Appendix

Translation of JP 6-232537 Supplied by Applicant

EXHIBIT I

[Translation]

(19) Japan Patent Office (JP) **(12) PATENT ISSUANCE REPORT (A)**

(11) Patent Application Release No.
Patent Release **Hei. 6-232537**

(43) Release date: August 19, 1994

(51) Int.Cl. [5]	Ident. Symbol	Office Control No.	F1	Technology Indicators
H 05 K 3/22	A	7511-4E		
H 01 L 21/82				
23/12				
		9169-4M	H 01 L 21/82	S
		9355-4M	23/12	Q

Examination requested: Not yet
Items in Application: 1 OL (Total 4 pages)

(21) Application No.: Patent Application Hei 5 [1993]-15411

(22) Application date: February 2, 1993

(71) Applicant: 000006231
Murata Works, Ltd.
26-10 Tenshin 2-chome, Nagaokakyo City
Kyoto Prefecture [Japan]

(72) Inventor: Masao Yonezawa
c/o Murata Works
26-10 Tenshin 2-chome, Nagaokakyo City
Kyoto Prefecture [Japan]

(72) Inventor: Akiyoshi Moriyasu
[same address]

(74) Agent: Kazuhide Okada, Patent Attorney

(54) **Name of Invention:** Method of Short-circuiting Electrode for Closed-circuit Formation

(57) **Summary**

Purpose: To reliably make short circuits in a method for short-circuiting electrodes used in forming paired closed circuits.

Makeup: In forming paired electrodes for making closed circuits in such form that the side where they are connected to the wiring pattern will be narrower than the wiring pattern, from atop these paired electrodes one imprints soldering paste in a region having an area greater than these electrodes, then heats this soldering paste and fuses it so that the above-noted paired electrodes are short-circuited by the fused solder.

Scope of Patent Application

Application Item 1 A method for short-circuiting electrodes used to form closed circuits that is character-ized by forming, on a substrate, paired electrodes for forming closed circuits so shaped that their side connected to the wiring pattern is narrower and they face each other across a prescribed gap; they are imprinted from atop the paired electrodes with solder paste in an region with an area larger than those electrodes; and by heating and fusing that solder paste the above-noted paired electrodes for forming closed circuits are short-circuited by the solder.

Detailed Explanation of Invention

0001 Field for Commercial Application This patent relates to a method for short-circuiting electrodes for forming the closed circuits used in the composite-circuit parts of hybrid ICs, etc.

0002 Usual Technology In composite circuit parts such as hybrid ICs, when—for instance—trying to trim resistors connected within closed circuits, one needs to be able to measure the resistance of a single resistor.

0003 However, when other resistors are connected in the closed circuit, the resistance of such a resistor will be affected and one cannot measure the resistance of the very resistor one is trying to trim, so that precise trimming is not possible.

0004 Due to that, one starts out with the resistor one seeks to trim cut off in the part of the wiring pattern forming the closed circuit so that it will not be affected by other resistors, and after that one connects the isolated part of the wiring pattern to form the closed circuit.

0005 Such means of forming closed circuits is a method long followed and is shown in Figure 3. I.e., as shown in Fig. 3(a), one forms paired rectangular electrodes 12,12 for a closed circuit connected to wiring patterns 11,11 on a substrate where a composite circuit part is to be formed. As that does not yet form a closed circuit, it is in a state where, for instance, trimming resistors is possible. Then, when the trimming is done, as shown in Fig. 3(b), one imprints soldering paste 13 from above with an area that encompasses paired electrodes 12. If one then heats and fuses soldering paste 13, electrodes 12, 12 for forming a closed circuit will be short-circuited by fused solder 14, as shown in Fig. 3(c), and the closed circuit will be formed.

0006 Issue the Invention Seeks to Resolve On the other hand, with the recent refining in the lead pitch of the electronic parts mounted on the substrates of integrated circuits, etc., soldering paste has been developed and put to use for such fine pitches to make short circuits unlikely between leads.

0007 And yet, because short circuits are unlikely with such soldering paste due to their nature even between the above-noted electrodes 12,12 for forming closed circuits, forming reliable closed circuits becomes difficult, giving rise to the problem that one must make corrections with each soldering.

0008 Hence, even when using the above-noted kind of soldering paste for fine pitch situations, with this invention the goal is to provide an electrode short-circuiting method for forming closed circuits such that the short-circuiting of these electrodes can be done reliably.

0009 Means to Resolve the Issue To attain such a goal, this invention's short-circuiting method for electrodes used for forming paired electrodes for making closed circuits is distinguished by making such electrodes in such form that the side where they are connected to the wiring pattern is narrower than the wiring pattern and from atop these paired electrodes one imprints soldering paste in a region with an area greater than these electrodes, then heats and fuses this soldering paste so that the above-noted paired electrodes are short-circuited by the fused solder.

0010 Effects By forming the paired electrodes for use in closed circuits in a shape where they are narrower on the wiring pattern side, face each other across a prescribed gap, and by imprinting soldering paste on a region with an area larger than those electrodes and then fusing that paste on the region's outer side where electrodes are narrower than the wiring pattern, drawing it toward the electrodes for closed circuits, it adheres uniformly to the electrode surfaces. So, the amount of fused solder near the electrode gap becomes greater, and one can easily get the paired electrodes short-circuited.

0011 Application example Below, we will explain an example of applying this invention, referring to the figures.

0012 First, as shown in Fig. 1(a), when forming the wiring pattern on a substrate, one simultaneously makes paired electrodes 2,2 for forming a closed-circuit, shaping them so that they are narrower at the side of wiring pattern 1,1 which is connected to that wiring pattern. This pair of electrodes are made facing each other across a gap for instance in the range of 100μm.

0013 Then, after completing such designated processing as trimming of resistors, one imprints from above solder paste 3, as shown in Fig. 1(b), for a fine pitch on a region with an area greater than paired electrodes 2,2 for a closed circuit.

0014 After that, one heats and fuses solder paste 3 so that it covers electrodes 2,2 and the region on the outer side of the narrow part of wiring pattern 1,1 for these electrodes so that it spreads out uniformly; and , as shown in Fig. 1(c), paired electrodes 2,2 will be shorted by the fused solder 4. Of course, this fused solder gradually cools and hardens.

0015 The shape of electrodes 2,2 for forming closed circuits may also be as shown in Figure 2 as long as their wiring-pattern side 1,1 is narrower. And, needless to say, by forming electrodes 2,2 as explained above there would be cases in which one uses the usual soldering paste as the short-circuiting will be done reliably.

0016 Effectiveness of Invention As will be clear from the above explanation, from having imprinted soldering paste from above over the electrodes as described with this invention, short-circuiting of the paired electrodes for making closed circuits will be done reliably.

Simple Explanation of Figures

Figure 1 is a figure to explain this invention's method of short-circuiting electrodes for making closed circuits. Fig. 1(a) is a plane diagram of the electrodes; Fig. 1(b) illustrates the condition when the soldering paste is imprinted from above the electrodes shown in Fig. 1(a); and Fig. 1(c) shows the conditions after the soldering paste shown in Fig. 1(b) has fused.

Figure 2 is a figure showing another shape of the electrodes used in this invention.

Figure 3 is a figure for illustrating the usual way of short-circuiting such electrodes. Fig. 3(a) is a plane figure of the electrodes for making closed circuits; Fig. 3(b) is a figure showing the condition when the soldering paste has been imprinted from above on the electrodes shown in Fig. 3(a); and Fig. 3(c) shows the conditions after the soldering paste has been fused.

Explanation of Symbols

1. 11 Wiring pattern
2. 12 Electrodes for forming closed circuits
3. Soldering paste
4. Fused solder

Related Proceedings Appendix

None Cited